# Uniform High Current Field Emission of Electrons from Si and CNF FEAs Individually Controlled by Si Pillar Ungated FETs

L. F. Velásquez-García[1], B. Adeoti[1,2], Y. Niu[1,2], and A. I. Akinwande[1,2]

[1]Microsystems Technology Laboratories [2]Electrical Engineering and Computer Science
Massachusetts Institute of Technology, Cambridge, MA, U.S.A.

## Abstract

We report the demonstration of the first dense ($10^6$ emitters / $cm^2$), high current (10 mA) array of individually ballasted field emitters that use vertical ungated field effect transistors (FETs) as current limiters. Each silicon or carbon nanofiber (CNF) emitter is individually connected in series with a silicon pillar ungated FET or current limiter (Fig. 1). The ungated FET takes advantage of the saturation of carrier velocity in silicon to obtain current source-like behavior – required for uniform and high current operation with small power dissipation.

## Introduction

Electrons are field emitted from the surface of metals and semiconductors when the potential barrier that holds electrons within the material (workfunction) is deformed by the application of a high electrostatic field [1]. High surface electrostatic fields are typically obtained by the application of a voltage to a high aspect ratio structure with nano-meter scale tip radius which usually has Gaussian or log-normal distribution [2]. Due to the exponential dependence on tip radius, emission currents are extremely sensitive to tip radii variation. Consequently, at a given voltage only a small fraction of the tips in an array emit electrons because the sharper tips would have burned-out, while the duller tips are yet to emit. Attempts to increase the emission current by increasing the voltage often result in burnout and shifting of the operating voltage to higher voltages. Therefore, it is difficult to obtain uniform or high currents from field emitter arrays (FEAs). Spatial non-uniformity can be substantially reduced if arrays of emitters are ballasted as demonstrated in the past [3]. However, ballasting of individual emitters has not been attempted due fabrication complexity. Ballasting individual emitters would prevent destructive emission from the sharper tips while allowing higher overall current emission because of emission of duller tips. The use of large resistors in series with the field emitters is an unattractive ballasting approach because of the resulting low emission currents and large power dissipation in the resistors (Fig. 2 A). MOSFETs can ballast the emission of FEAs [4], but this approach is unable to yield high density FEAs because the MOSFETs consume considerable area if implemented as individual ballasts. A better approach for ballasting field emitters is the use of vertical un-gated field effect transistors that effectively provide high dynamic resistance with large saturation currents (Fig. 2 B).

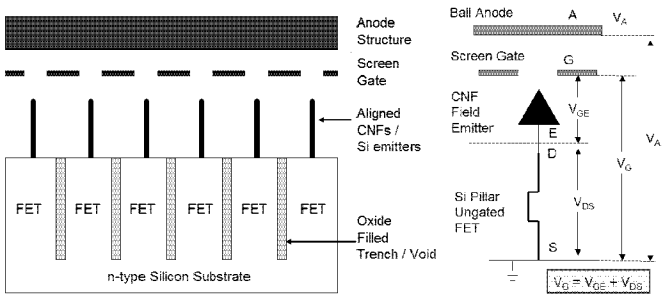


Fig. 1. Device Structure (left) and equivalent circuit (right). FEs are formed on top of Si columns (FETs). Each column holds one emitter. Drain of the FET is connected to the emitter of the FE i.e. node floating. Voltage is distributed between FE and FET.

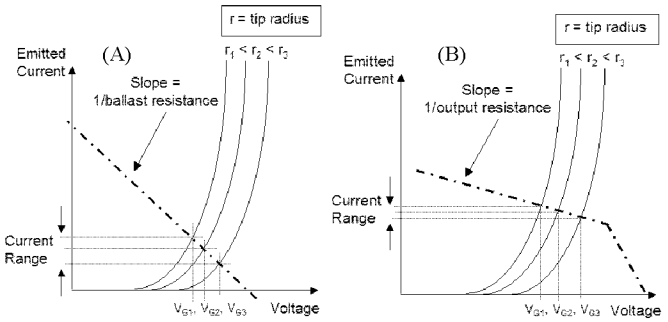


Fig. 2. Ballasting of FEAs using resistors (A) and ungated FETs (B). In the first case, emission uniformity is achieved at the expense of low emission currents and large power dissipation. In the second case, output resistance provides high impedance resulting in large emission currents and low power dissipation.

## Device Analysis, Modeling and Simulation

We developed a model to quantify emission current sensitivity of field emitters to tip radii and workfunction variation. The model also examined the influence of ballasting by resistors and ungated FETs on emission current variation. Based on this analysis, parameters for the ungated FET were calculated (Fig. 3 – 4). Structural parameters of the ungated FET were determined through process and device simulations that explored channel doping between $10^{13}$ $cm^{-3}$ and $10^{16}$ $cm^{-3}$ and channel length between 10 μm and 100 μm with a cross-section area of 1 μm x 1μm. Current source-like behavior is obtained because of velocity saturation at high fields (Fig. 5).

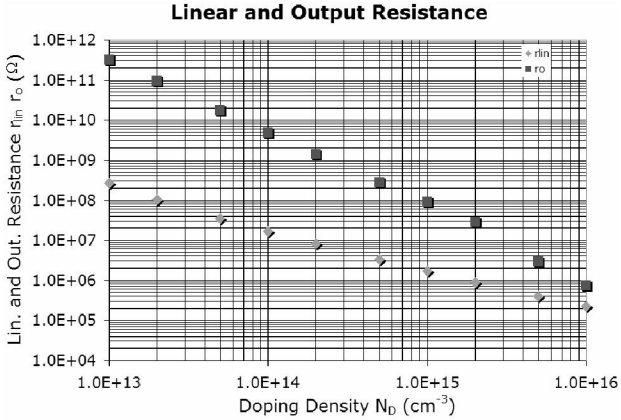


Fig. 3. Ungated FET simulation –linear ($r_{lin}$) and output impedance ($r_o$) vs. doping concentration.

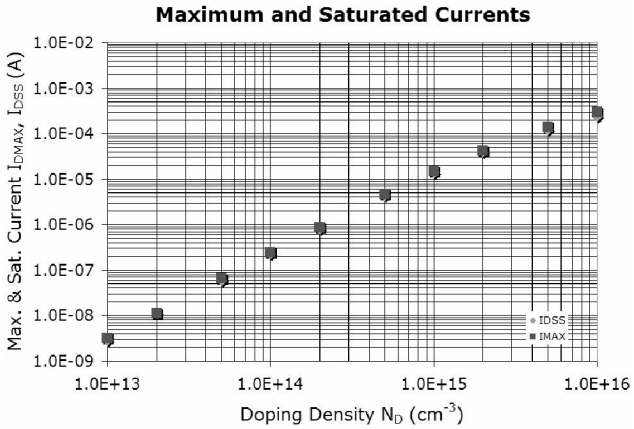


Fig. 4. Ungated FET simulation –maximum ($I_{MAX}$) and saturated ($I_{DSS}$) currents vs. doping concentration.

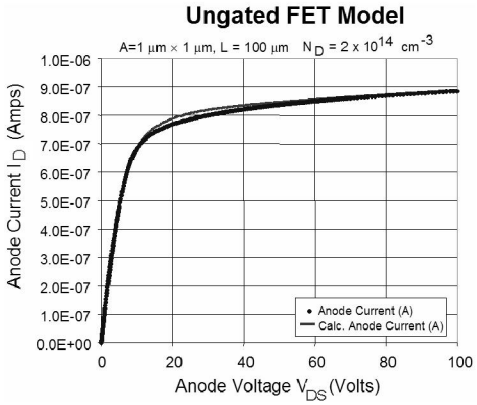


Fig. 5. IV characteristics of ungated FET –analytical model and simulated performance. The simulations match the proposed reduced-order model. Current saturates for large enough voltage.

The simulated IV characteristics of the ungated FET closely matches the proposed analytical model

$$I_D = g_{LIN} V_{DS} \left[1 + \frac{V_{DS}}{V_A}\right] \Bigg/ \sqrt{1 + \left(\frac{V_{DS}}{V_{DSS}}\right)^2} \qquad (1)$$

where $I_D$ is the drain current, $g_{LIN}$ is the linear conductance, $V_{DS}$ is the drain-to-source voltage, $V_{DSS}$ is the drain-to-source saturation voltage (velocity saturation), and $V_A$ is the early voltage (channel length modulation). Simulation of the field emitter integrated with the ungated FET show that the emission current could be maintained within 5% of the target value for a 6-σ tip radii variation (Fig. 6 - 7).

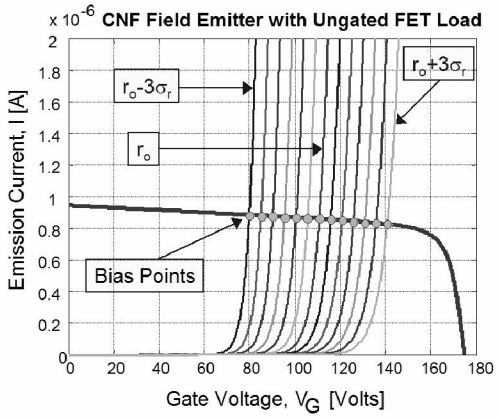


Fig. 6. Simulation of integrated device FET/FE –sensitivity to ± 3-σ tip radii variation.

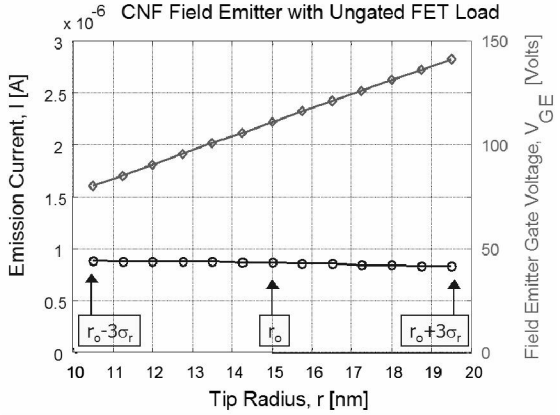


Fig. 7. Simulation of integrated device FET/FE –Current control over ± 3-σ radii tip variation.

## Device Fabrication

Un-gated FETs were fabricated on n-Si by depositing a dielectric thin film stack (0.5 μm PECVD $SiO_2$/0.5 μm LPCVD silicon-rich silicon nitride/ 0.5 μm thermal $SiO_2$), followed by contact photolithography, RIE of the thin film stack, DRIE of the n-Si (Fig. 8), wet oxidation, and HF release in special chamber (Fig. 9). Si FEAs were fabricated by modifying the DRIE step of the un-gated FET (tip sharpening occurs at the oxidation step, Fig. 10) while PECVD CNF FEAs are fabricated by replacing the thin film stack previously described by a Ni/TiN structure and using RIE to pattern the TiN and wet etching to pattern the Ni film (Fig. 11). CNFs were grown using the Ni pads as catalyst in a PECVD reactor that uses ammonia and acetylene [5].

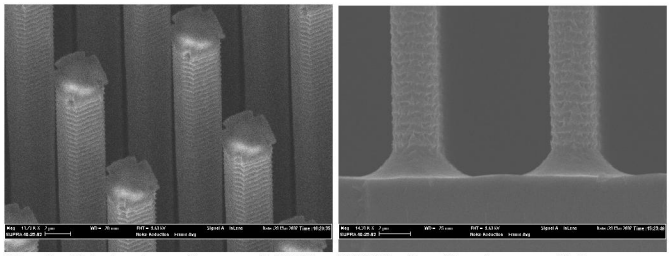

Fig. 8. Fabrication of ungated FETs –DRIE of n-Si substrate. Columns are 100 µm tall and 3.5 µm wide. DRIE scalloping is noticeable (left). Column roots are properly chamfered for mechanical high performance (right).

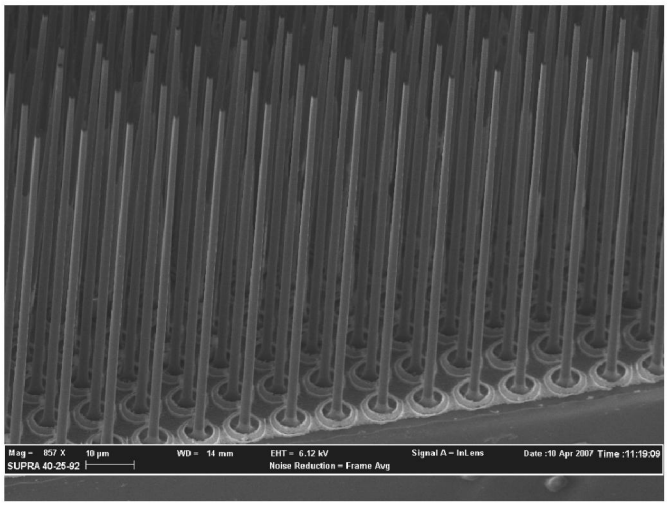


Fig. 9. Fabrication ungated FETs –Si Pillar thinning. Wet oxidation is used to reduce the columns width. Columns are 100 µm tall and less than 1.0 µm wide. HF vapors are used to remove the thermal oxide.

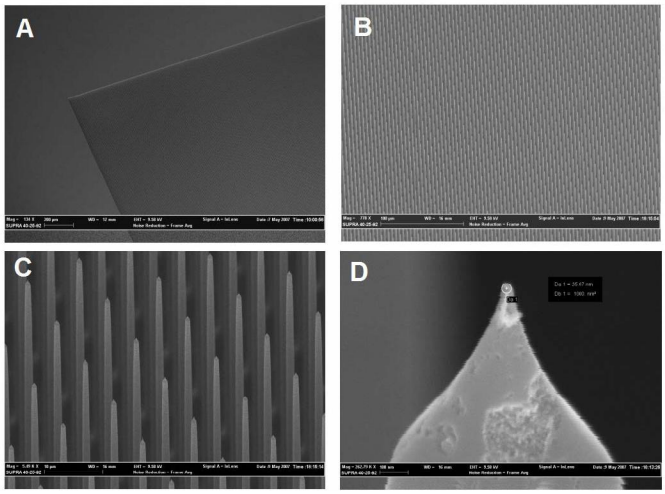


Fig. 10. Fabricated Si FEAs. A) A 1 cm × 1 cm Si FEA on top of 100 µm-tall silicon columns, 10 µm column pitch; B) Zoom of the Si FEA; C) a few Si FE on top of ungated FETs; D) Si tip -tip diameter equal to 35 nm.

To test the un-gated FETs, the structures shown in Fig. 9 received PECVD oxide deposition (to isolate the FETs) followed by BOE dip (to expose the top of the FETs) and Al/Ti metallization (Fig. 12). The samples were annealed at 380 °C in a forming gas atmosphere.

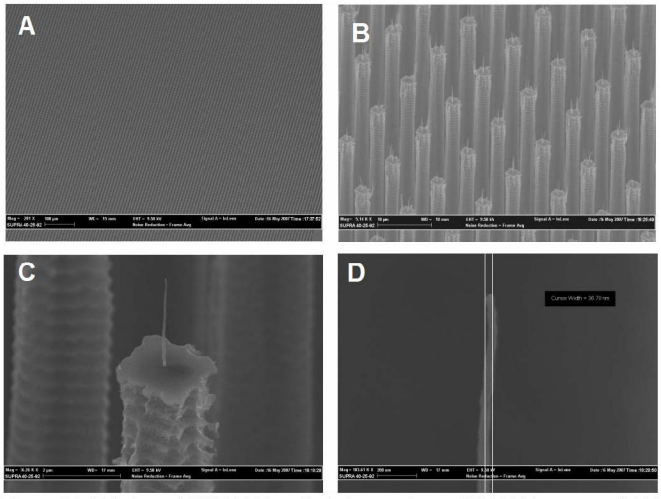


Figure 11. Fabricated CNF FEAs. A) A 1 cm × 1 cm CNF FEA on top of 100 µm-tall silicon columns, 10 µm column pitch; B) a local isolated CNF FEA on top of ungated FETs; C) An isolated 4 µm-tall CNF on top of ungated FET; D) CNF tip –tip diameter equal to 36 nm.

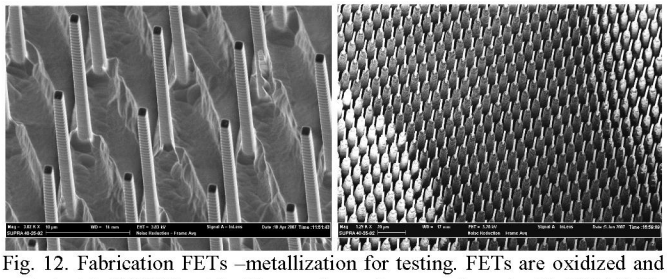

Fig. 12. Fabrication FETs –metallization for testing. FETs are oxidized and coated with PECVD oxide. Then, column tips are released with BOE (left). Al/Ti is sputtered to FETs using a shadow mask with a grid pattern to make electrical contact for testing (right).

## Device Characterization

Ungated FET characteristics show current source-like behavior consistent with device simulation (Fig. 13). For a doping concentration of $10^{15}$ cm$^{-3}$ a linear conductance $g_{LIN}$ of to 2 µS is experimentally obtained while simulations predict a value equal to 0.6 µS. The saturation voltage $V_{DSS}$ is estimated at 30 V, in good agreement with the simulations. Simulations also predict an output resistance $r_o$ equal to 100 MΩ, while experimentally a flat IV profile is obtained for voltages substantially larger than $V_{DSS}$. However, the experimental data show some non-ideal characteristics such as poor ohmic contact resistance (related to the way the metallization was conducted) and negative output conductance at medium voltages. Small arrays (60 x 70) of the integrated device fabricated on 150-250 Ω-cm n-Si substrates show that emission currents saturate at high voltages due to ballasting of the ungated FETs (Fig. 14). The emission current per tip is consistent with the saturation currents of the ungated FET. We also characterized large arrays ($10^6$ emitters) of the integrated device and an emission current of 10 mA was demonstrated (Fig. 15). The emission current was only limited by the compliance of the equipment

and device power dissipation. We speculate that tests in pulse mode, low duty cycle, would yield larger currents, and therefore, demonstration of ballasting in the larger array.

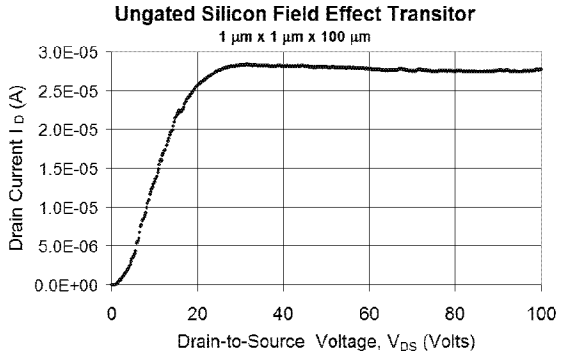


Fig. 13. FET Characterization –current saturation is achieved. Doping concentration is $10^{15}$ $cm^{-3}$. Simulations predict saturation slope of 0.6 μS, consistent with experimental data (2 μS are obtained).

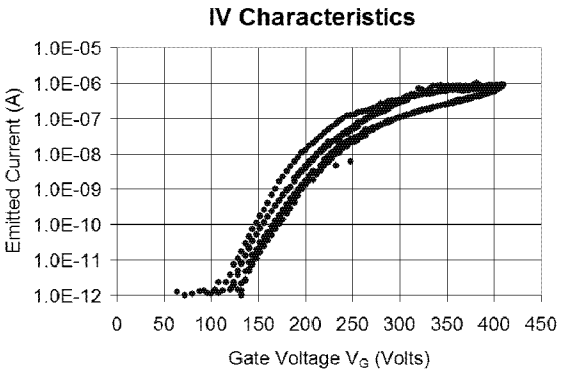


Fig. 14. Integrated FET/FEA testing –Saturation current is achieved (flattening of IV characteristics). A smaller array (60 ×70 tips) made with 150 – 200 Ω-cm n-Si was used to circumvent the testing rig limitations.

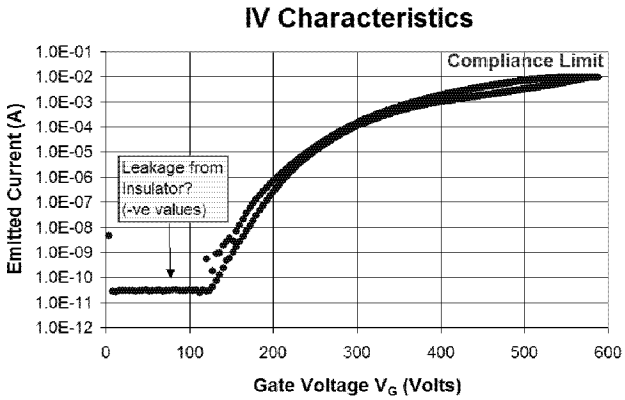


Fig. 15. Integrated FET/FEA testing. High field emission current is achieved. (10 mA). At large voltages some current saturation occurs. Extracted tip radii from FN plot is consistent with SEMs (40 nm radius).

## Conclusions

We demonstrated the first dense ($10^6$ emitters), high current (10 mA) array of individually ballasted field emitters that use ungated FETs as current limiters. The results show that the emission current is limited by the ballasting ungated FETs. This work represents four key contributions: (1) Vertical ungated FETs with high aspect ratio (length-to-column width > 100) were fabricated, tested, and clearly demonstrated current saturation and that vertical FETs enable large FEA density. (2) Isolated PECVD CNFs / Si tips were formed on top of high aspect ratio Si columns allowing FEs to be individually ballasted. (3) The integrated device produced the highest reported field emitted current from silicon. (4) The device demonstrates a method for ballasting high current FEAs using the saturation velocity of electrons at high fields.

## Acknowledgements

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